WHAT IS CLAIMED IS:

1. A base pad layout for reducing the parasitic base-collector capacitance, comprising:

a base region which is aligned in a <01$\bar{1}$> or <011> orientation with respect to the semiconductor substrate;

a base pad region which has a fixed slope with respect to said base region; and

a base feeding region which is aligned in a <010> orientation and connects said base region and said base pad region.

2. The base pad layout as claimed in Claim 1, wherein said base pad region is in a square or rectangular shape.

3. A method for fabricating a triple mesa HBT using the base pad layout, comprising the processing steps of:

a first process for isolating a base region and a base pad region and forming a base pad layout by connecting said regions to a base feeding region;

a second process for sequentially stacking a sub-collector InGaAs layer/an etching stopper lnP layer/ a base-collector lnGaAs layer/an emitter lnP layer/ an emitter cap lnGaAs layer on a semi-insulating lnP

substrate using the epitaxy growth method;

a third process for depositing a base metal using said base pad layout as a mask after depositing a emitter metal on the epitaxy structure formed in said second process and sequentially etching the emitter cap lnGaAs layer and the emitter lnP layer to allow said emitter metal to self-align and to expose the upper side of the base-collector lnGaAs layer;

a fourth process for defining a first photoresist to some parts of the base region and the base feeding region in order to protect an emitter region;

a fifth process for forming a void area underneath the base feeding region using side etching after exposing the upper side of the sub-collector lnGaAs layer by etching the base-collector lnGaAs layer and the etching stopper lnP layer using said first photoresist and base metal layer as a mask;

a sixth process for depositing a collector metal on said sub-collector lnGaAs layer; and

a seventh process for defining a second photoresist in order to protect the lower part of the emitter and the base region and removing said second photoresist after isolating the base region and the base pad region by side etching the sub-collector lnGaAs layer.

4. The method as claimed in Claim 3, wherein said etching in the fifth and seventh process involves a

side etching of the lower part of the base feeding region using the anisotropic etching characteristic where the etching speed varies according to the crystal lattice direction.

5. The method as claimed in Claim 3, wherein said etching in the fifth and seventh process involves a side etching of the lower part of the base feeding region using an etchant H3PO4: H2O2: H2O for the InGaAs layer and an etchant HCl: H3PO4 for the InP layer.

6. The method as claimed in Claim 3, wherein the etching speed in the fifth and seventh process is dependent upon the type of etchant, concentration and temperature used.

7. The method as claimed in Claim 3, wherein said lower part of the base feeding region undergoes a etching of the whole epitaxy structures except the semi-insulating lnP substrate in order to reduce the base-collector capacitance.

8. The method as claimed in Claim 3, wherein if said HBT is a double HBT, then InGaAs layer becomes a base layer and the lnP layer becomes a collector layer.

9. The method as claimed in Claim 4, wherein the etching speed in the fifth and seventh process is dependent upon the type of etchant, concentration and temperature used.

10. The method as claimed in Claim 5, wherein the etching speed in the fifth and seventh process is dependent upon the type of etchant, concentration and temperature used.